US-PAT-NO: 5388328
DOCUMENT-IDENTIFIER: US 5388328 A
TITLE: Process for fabricating an interconnected multilayer board

DATE-ISSUED: February 14, 1995

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
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ASSIGNEE INFORMATION:

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APPL-NO: 8/ 187546

DATE FILED: January 28, 1994
PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application is a divisional of application Ser. No. 08/037,543, filed on Mar. 22, 1993, now U.S. Pat. No.

5,300,735, issued on Apr. 5, 1994, which application is a continuation of
application Ser. No. 07/672,117, filed on Mar. 19, 1991, (now abandoned).

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FIELD-OF-SEARCH: 428/901;29/829 ;29/846 ;29/830 ;29/825 ;29/852 ;156/902
;174/267

REF-CITED:

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al.

ART-UNIT: 326

PRIMARY-EXAMINER: Arbes; Carl J.

ATTY-AGENT-FIRM: Antonelli, Terry, Stout & Kraus

ABSTRACT:
A process for the fabrication of an interconnected

multilayer board involves
the steps of forming a metallic under-conductive layer on a base substrate,
forming a windowed resist layer on the metallic under-conductive layer, filling
windows of the resist layer with a conductor by plating thereby forming a
conductor layer, forming another windowed resist layer on the conductor layer
and filling windows of this resist layer with a conductor by plating, thereby
forming a via-hole layer and to provide a two-level structure of the conductor
layer and the via-hole layer. Thereafter, the resist layers and portions of
the metallic under-conductor layer other than those in contact with a lower
face of the conductor constituting the conductor layer are dissolved to form a
two-level skeleton structure of conductor lines and spaces within the skeleton
structure are filled with a varnish in a solventless form and the varnish is
cured.

64 Claims, 70 Drawing figures